**IN THE SPECIFICATION**

Please amend the specification as follows:

Page 2, line 20, delete "SUMMARY OF THE INVENTION".

Page 3, line 9, insert --SUMMARY OF THE INVENTION--.

Please replace the paragraphs beginning on page 5 through page 6, line 13, with the following rewritten paragraphs as follows:

-- Fig. 1 shows a shared memory multiprocessor system representing a first embodiment of the present invention. The multiprocessor system includes sixty-four nodes 100, ···, 200 and an inter-node network 900. All nodes have the same structure. Node 100 includes a plurality of CPUs 110, 111, ···, 112 and a main memory 160. Transactions to the node 100 from ~~he~~ the network 900 are received by a network transaction receiver 151. Transactions from the node 100 to other nodes are transmitted by a network transaction transmitter 157.

Main memory 160 is a part of a common main memory of the overall system. In other words, the main memory of each node can be used by all of the CPUs within the overall system. That is a basic feature of a shared memory multiprocessor system. CPUs in the node 100 are connected to each other through a local bus 120. However, other types of ~~connection~~ connections such as one to one connections or switches, can be employed instead of the local bus 120. Main memory access circuit 161 issues a network transaction for cache coherence check (CCC), when a main memory access request is issued from a local CPU, and also issues a main memory access transaction to another node. Further, the main memory access circuit 161 executes a main memory access on the local main memory 160, and also

executes CCC transactions and main memory access transactions received from other nodes. --

Please replace the paragraphs beginning on page 8 through page 10, line 9, with the following rewritten paragraphs as follows:

-- Fig. 4 and Fig.4 and Fig. 5 ~~illustrates~~ illustrate the data format of a transaction on a local bus and on the inter-node network, respectively. Respective transactions include a destination designation 2001, 3001, command species and source node number 2002, 3002, physical address 2003, 3003 and virtual page number 2004, 3004. The transaction shown in Fig. 4 is a transaction requesting a data transfer or requesting a cache data invalidation, which does not include data. Transaction shown in Fig. 5 is a transaction requesting writing back of a cache line or the sending of data in response to a data transfer request, which includes data 3005-3006. Maintaining data coherency among processors, cache memories, and partial main memories can be attained by the transactions of those different species.

(3) Operations of a memory access requesting node

A memory access from a local CPU is issued on the local bus 120 with an access destination physical address. The physical address is obtained by referring to a TLB (Translation Lookaside Buffer) in the local CPU. The bus transaction receive and distribute circuit 131 ~~receive~~ receives transactions on the local bus 120 and determines the transaction species. When a received transaction is a memory access transaction, the circuit 131 will send the physical address to the local/remote determination circuit 132 via signal line 132a. If the local/remote determination circuit 132 determines that the

physical address is in the main memory 160 of the local node, the circuit 131 will send the transaction to the main memory access circuit 161 via signal line 131 b and send the transaction to the virtual page number check circuit 142 via signal line 131c. The virtual page number check circuit 142 will read out a virtual page number and condition bit, using the access destination physical address of the transaction, from the physical page map table (PPT) 141 shown in Fig. 3 Then, the circuit 142 will check the read out virtual page number to determine whether it is coincident with the virtual page number address of the transaction or not. If the read-out virtual page number is coincident with the virtual page number address of the transaction and the condition bit indicates "valid", the circuit 142 will inform the main memory access circuit 161 of a "PPT hit", which means that the memory access transaction is valid. The main memory access circuit 161 executes the memory access corresponding to the memory access transaction, when a "PPT hit" is indicated. According to the status of the memory line to be accessed or to the transaction species, the procedure includes a read or write access of main memory 160 and the issue of a network transaction for maintaining cache coherency. –